

General Description

The WSD30L120DN56 is the highest performance trench P-Ch MOSFET with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications.

The WSD30L120DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V _{DS}	Drain-Source Voltage	-30		V
V _{GS}	Gate-Source Voltage	±20		V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ -10V ¹	-120		A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ -10V ¹	-76		A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ -10V ¹	-27	-22	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ -10V ¹	-24	-19	A
I _{DM}	Pulsed Drain Current ²	-400		A
EAS	Single Pulse Avalanche Energy ³	324		mJ
I _{AS}	Avalanche Current	-36		A
P _D @T _C =25°C	Total Power Dissipation ⁴	78		W
P _D @T _A =25°C	Total Power Dissipation ⁴	6.8	6.25	W
T _{STG}	Storage Temperature Range	-55 to 150		°C
T _J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	55	°C/W
R _{θJA}	Thermal Resistance Junction-Ambient ¹ (t ≤ 10s)	---	20	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	1.6	°C/W

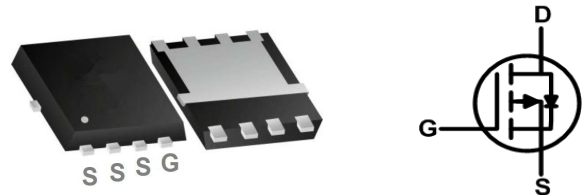
Product Summary

BVDSS	R _{DS(on)}	I _D
-30V	3.6mΩ	-120A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

DFN5X6-8 Pin Configuration



Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.0232	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-30A	---	2.9	3.6	mΩ
		V _{GS} =-4.5V, I _D =-10A	---	5.0	6.8	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.2	-1.5	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.6	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	---	---	-5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-30A	---	28	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2	5	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-15V, V _{GS} =-10V, I _D =-30A	---	135	---	nC
Q _{gs}	Gate-Source Charge		---	12	---	
Q _{gd}	Gate-Drain Charge		---	36	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, V _{GEN} =-10V, R _G =6Ω I _D =-1A, R _L =15Ω	---	22	---	ns
T _r	Rise Time		---	25	---	
T _{d(off)}	Turn-Off Delay Time		---	163	---	
T _f	Fall Time		---	104	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	6100	---	pF
C _{oss}	Output Capacitance		---	1130	---	
C _{rss}	Reverse Transfer Capacitance		---	1110	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	V _{DD} =-25V, L=0.5mH, I _{AS} =-36A	300	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,6}	V _G =V _D =0V, Force Current	---	---	-40	A
I _{SM}	Pulsed Source Current ^{2,6}		---	---	-400	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1	V
t _{rr}	Reverse Recovery Time	I _F =-15A, dI/dt=100A/μs,	---	32	---	nS
Q _{rr}	Reverse Recovery Charge	T _J =25°C	---	16	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, t<10sec.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.5mH, I_{AS}=-36A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

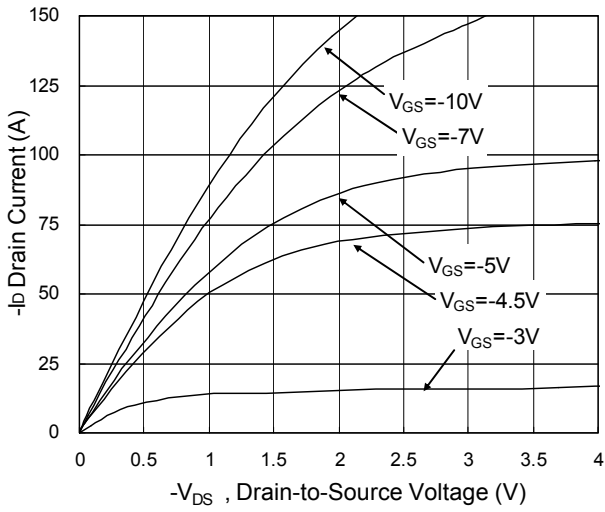


Fig.1 Typical Output Characteristics

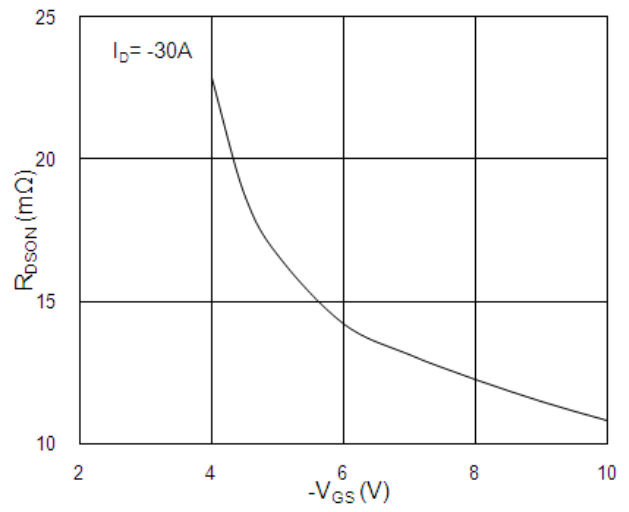


Fig.2 On-Resistance vs. G-S Voltage

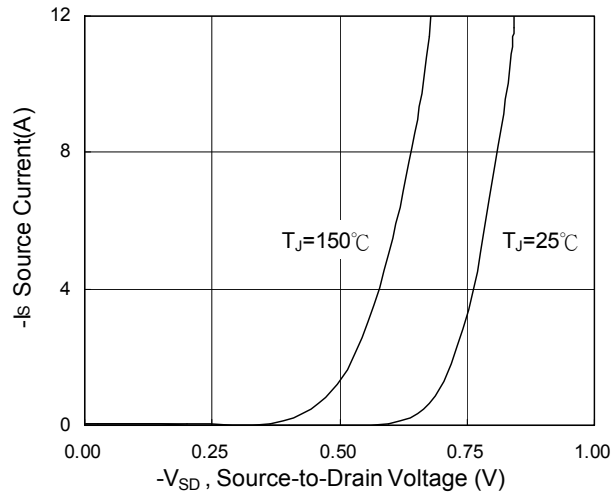


Fig.3 Forward Characteristics of Reverse

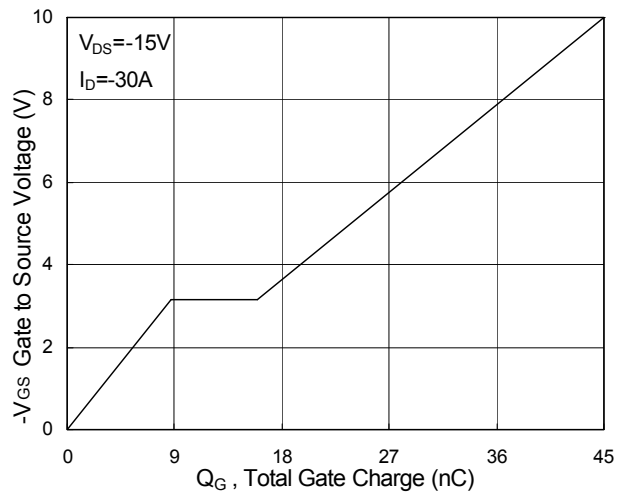


Fig.4 Gate-Charge Characteristics

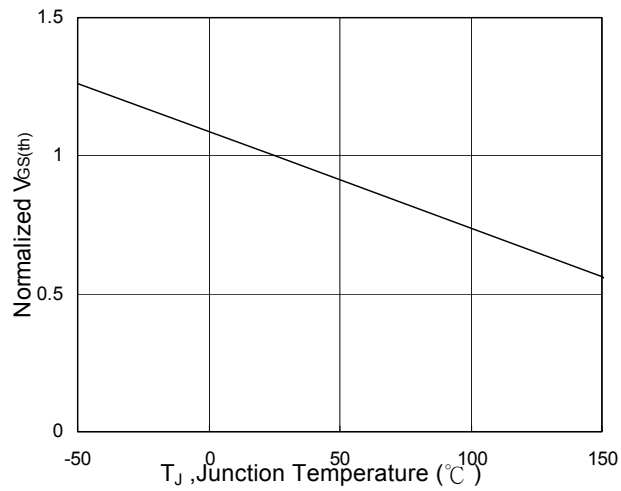


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

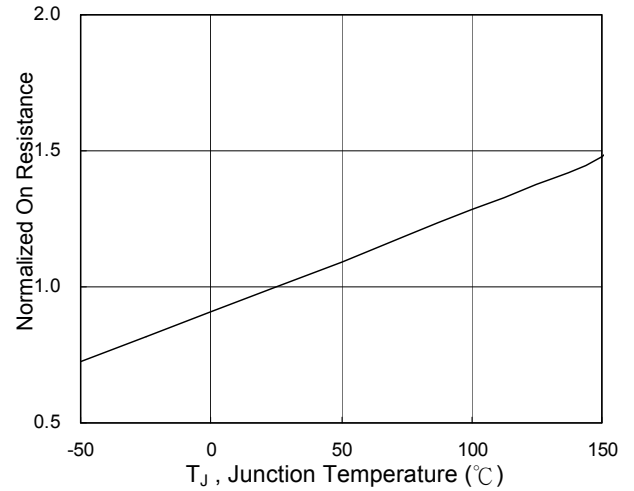


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

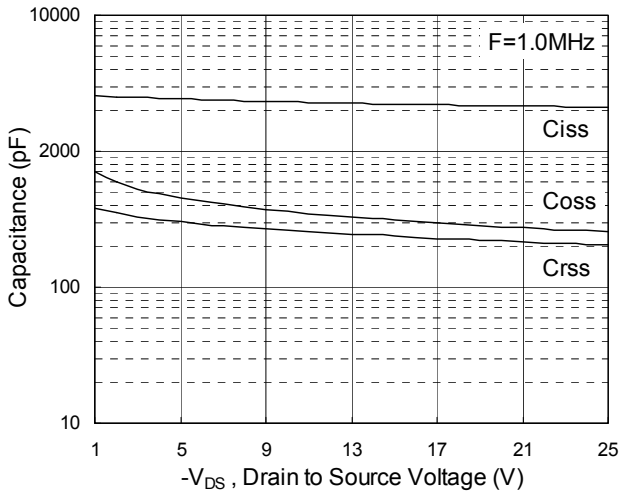


Fig.7 Capacitance

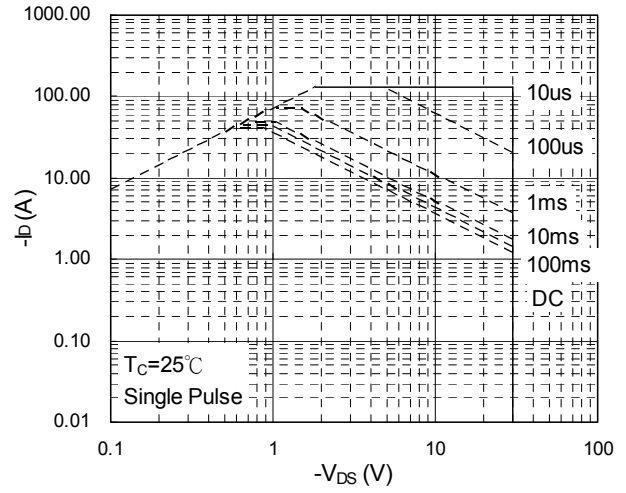


Fig.8 Safe Operating Area

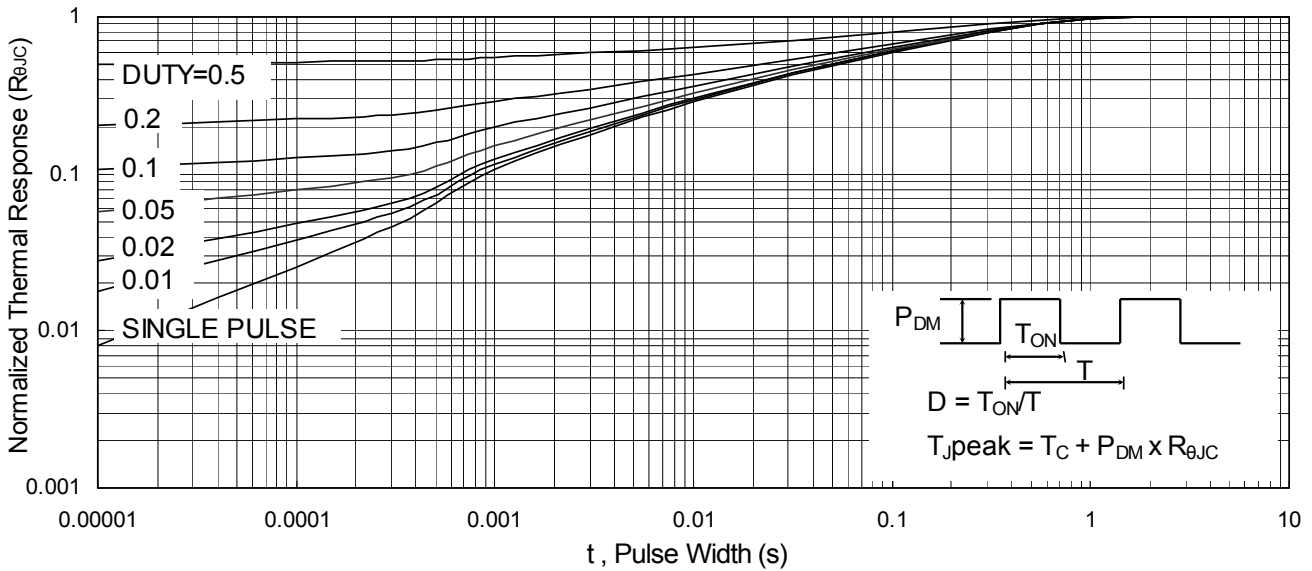


Fig.9 Normalized Maximum Transient Thermal Impedance

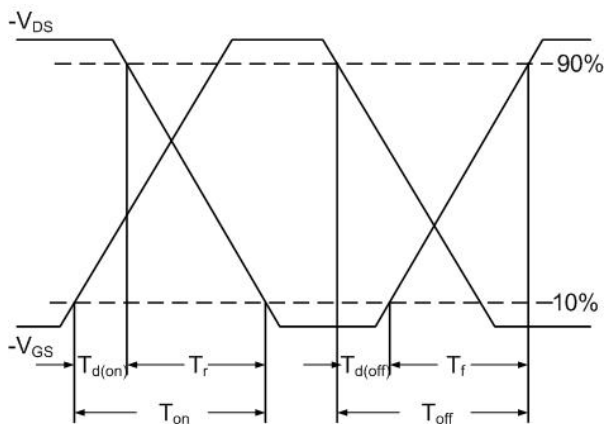


Fig.10 Switching Time Waveform

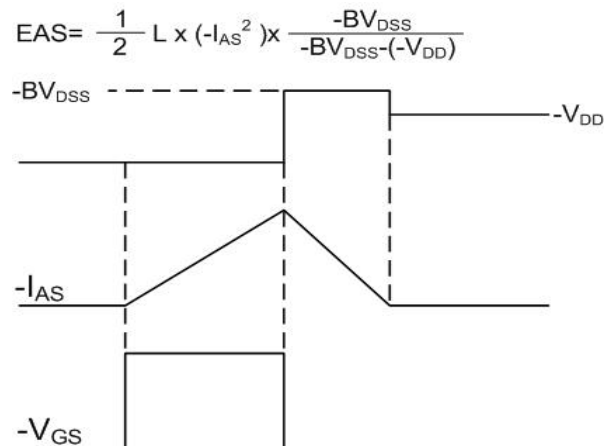


Fig.11 Unclamped Inductive Switching Waveform



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